Moritz Lipp (@mlqxyz)

Michael Schwarz (@misc0110)

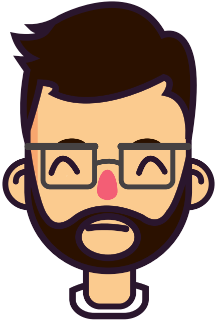
Daniel Gruss (@lavados)

Meltdown

Basics, Details, Consequences

Black Hat USA 2018
9 August, 2018 - Las Vegas, NV, USA

Who am I?



Moritz Lipp

PhD student @ Graz University of Technology

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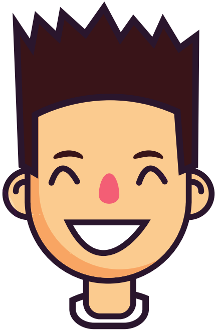

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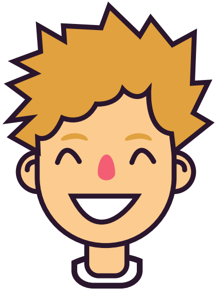

Daniel Gruss

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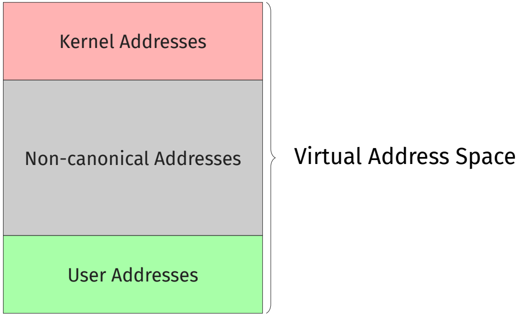
Team

- Anders Fogh
- Daniel Genkin
- Werner Haas
- Mike Hamburg
- Jann Horn
- Paul Kocher
- Stefan Mangard
- Thomas Prescher
- Yuval Yarom

Let’s Read Kernel Memory from User Space!

Virtual Memory

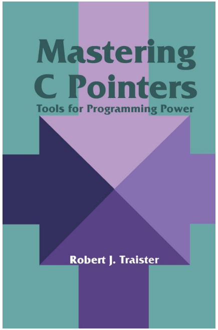


Building the Code

- Find something human readable, e.g., the Linux version

```
# sudo grep linux_banner /proc/kallsyms
ffffffff81a000e0 R linux_banner
```

Building the Code



```
char data = *(char*) 0xffffffff81a000e0;
printf("%c\n", data);
```

Building the Code

- Compile and run

Building the Code

- Compile and run

```
segfault at ffffffff81a000e0 ip 0000000000400535
      sp 00007ffce4a80610 error 5 in reader
```

Building the Code

- Compile and run

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segfault at ffffffff81a000e0 ip 0000000000400535
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- Kernel addresses are of course not accessible

Building the Code

- Compile and run

```
segfault at ffffffff81a000e0 ip 0000000000400535
      sp 00007ffce4a80610 error 5 in reader
```

- Kernel addresses are of course not accessible
- Any invalid access throws an exception → segmentation fault

Building the Code

- Just catch the segmentation fault!

Building the Code

- Just catch the segmentation fault!
- We can simply install a signal handler

Building the Code

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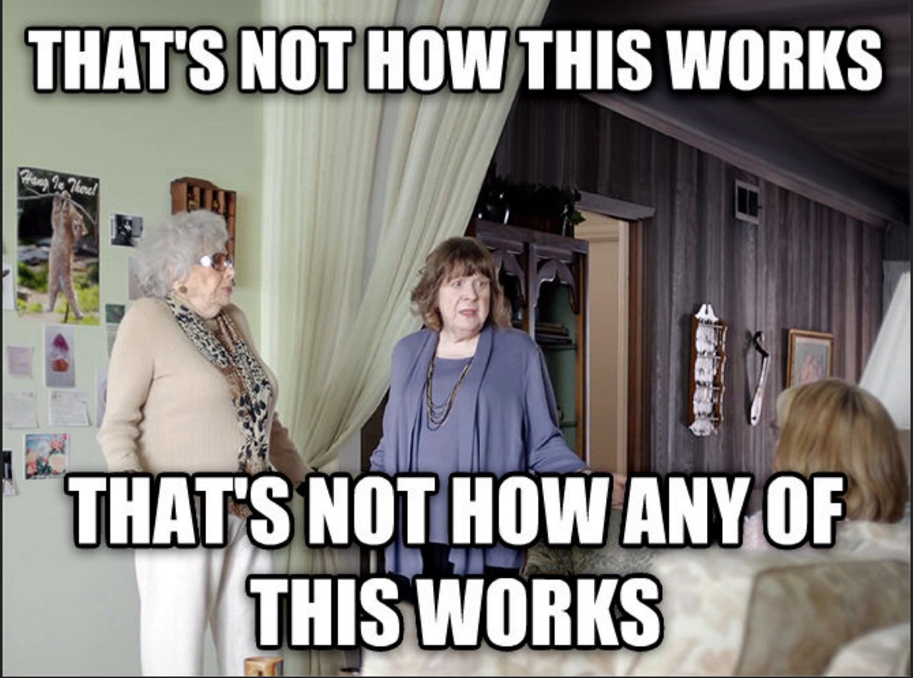
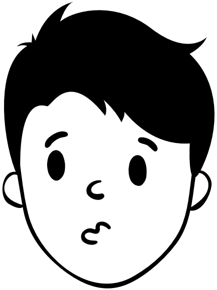
- We can simply install a signal handler
- And if an exception occurs, just jump back and continue

Building the Code

- Just catch the segmentation fault!
- We can simply install a signal handler
- And if an exception occurs, just jump back and continue
- Then we can read the value

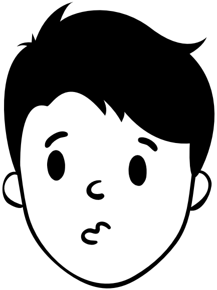

THAT'S NOT HOW THIS WORKS
Hang In There!
THAT'S NOT HOW ANY OF THIS WORKS

Building the Code



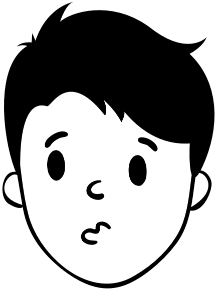
- Still no kernel memory

Building the Code



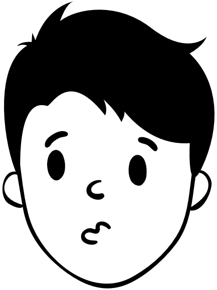
- Still no kernel memory
- Privilege checks seem to work

Building the Code



- Still no kernel memory
- Privilege checks seem to work
- Maybe it is not that straight forward

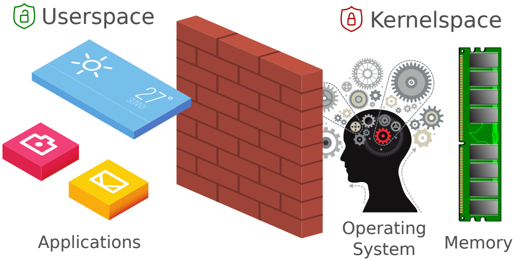
Building the Code



- Still no kernel memory
- Privilege checks seem to work
- Maybe it is not that straight forward
- Back to the drawing board

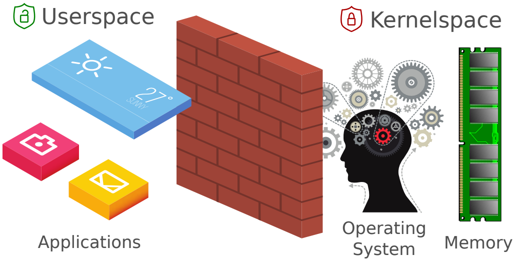
Operating Systems 101

Memory Isolation



- Kernel is isolated from user space

Memory Isolation



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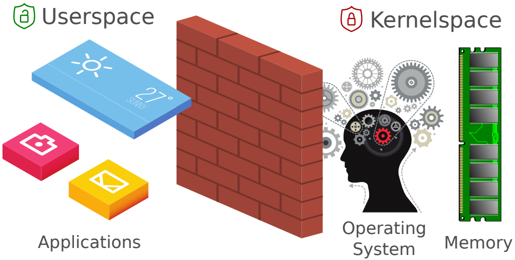
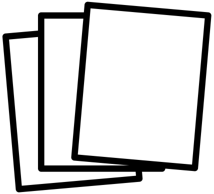
- This isolation is a combination of hardware and software

Memory Isolation



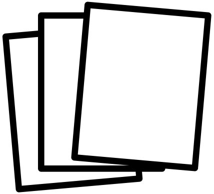
- Kernel is isolated from user space
- This isolation is a combination of hardware and software
- User applications cannot access anything from the kernel

Paging



- CPU support virtual address spaces to isolate processes

Paging

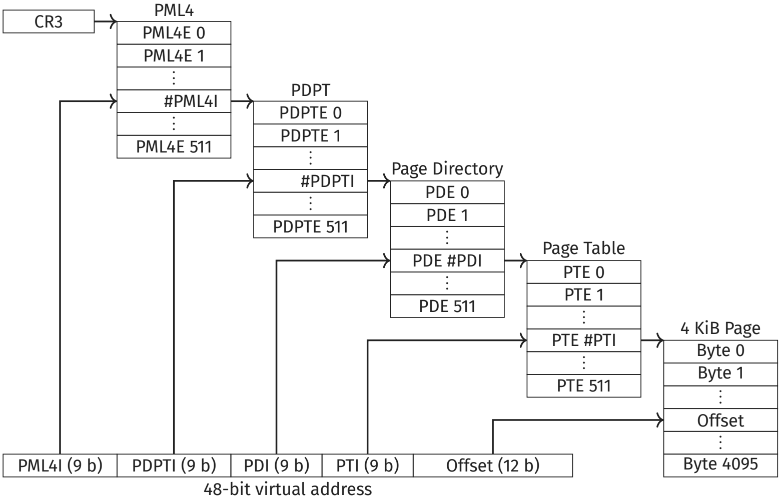


- CPU support virtual address spaces to isolate processes
- Physical memory is organized in page frames

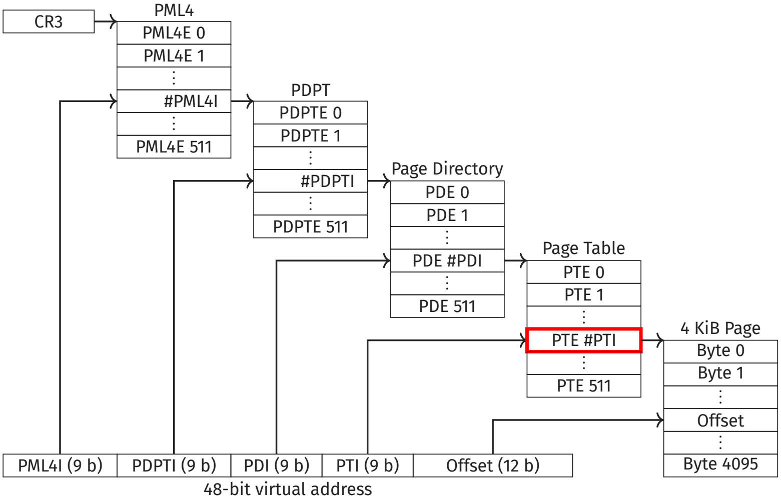
Paging

- CPU support virtual address spaces to isolate processes
- Physical memory is organized in page frames
- Virtual memory pages are mapped to page frames using page tables

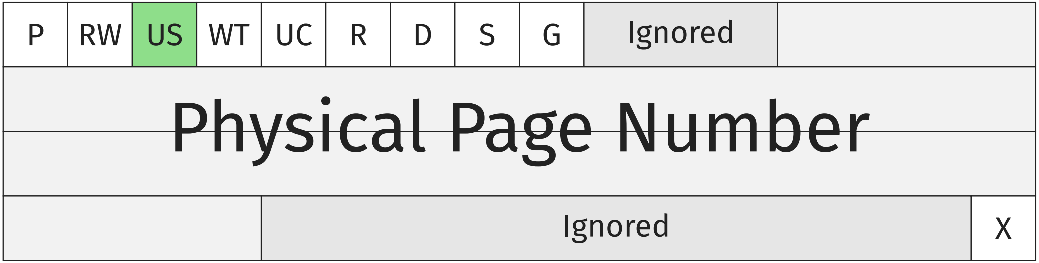
Address Translation on x86-64



Address Translation on x86-64



Page Table Entry



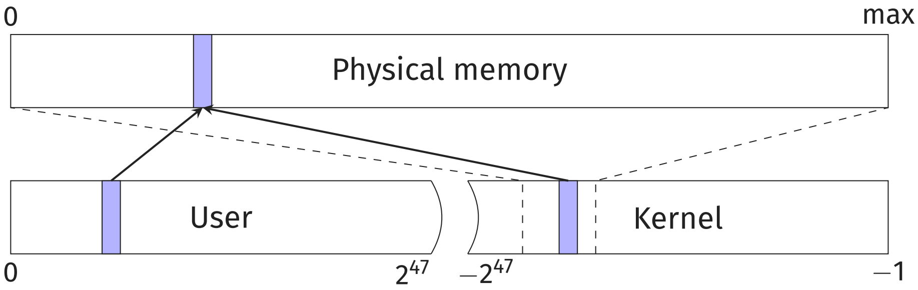
P | RW | US | WT | UC | R | D | S | G | Ignored

Physical Page Number

Ignored | X

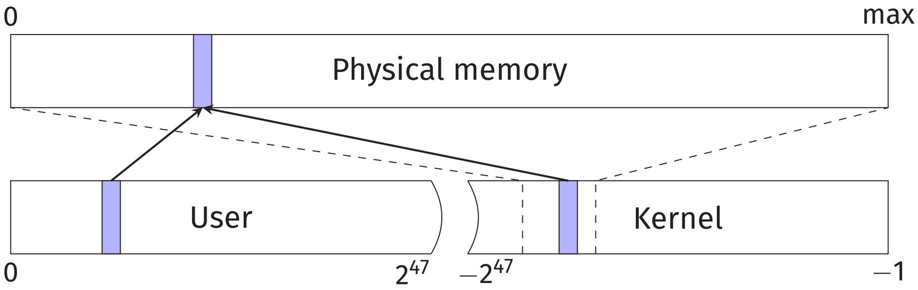
- User/Supervisor bit defines in which privilege level the page can be accessed

Direct-physical map



- Kernel is typically mapped into every address space

Direct-physical map



- Kernel is typically mapped into every address space
- Entire physical memory is mapped in the kernel

Loading an address

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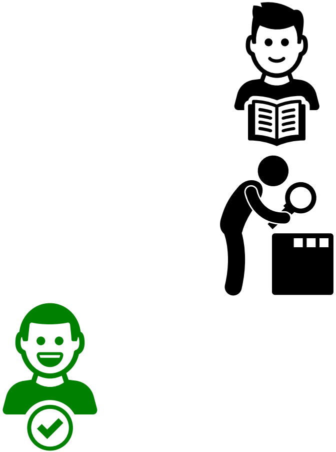

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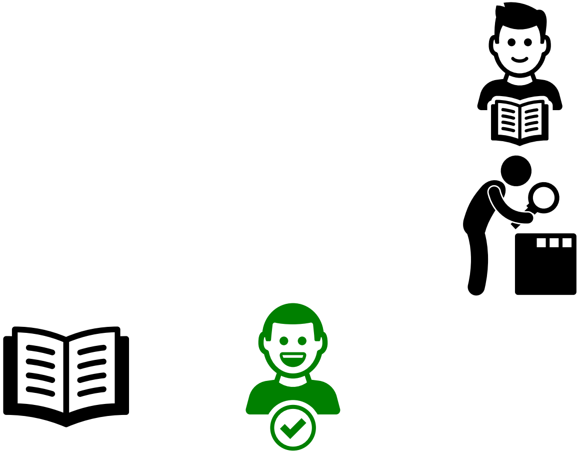

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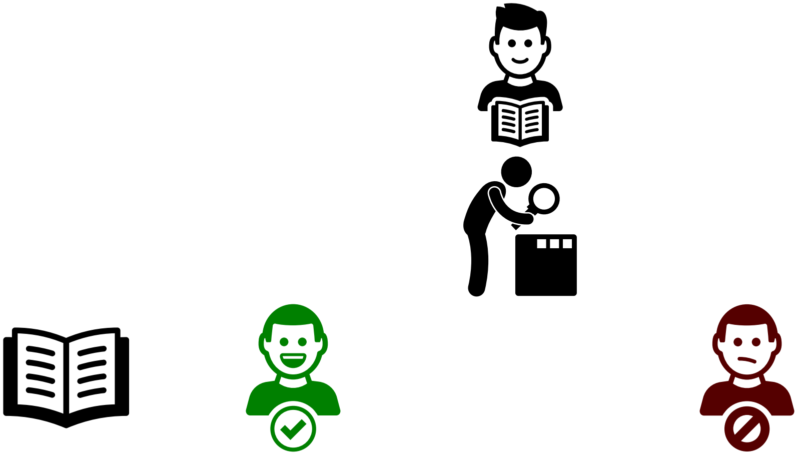

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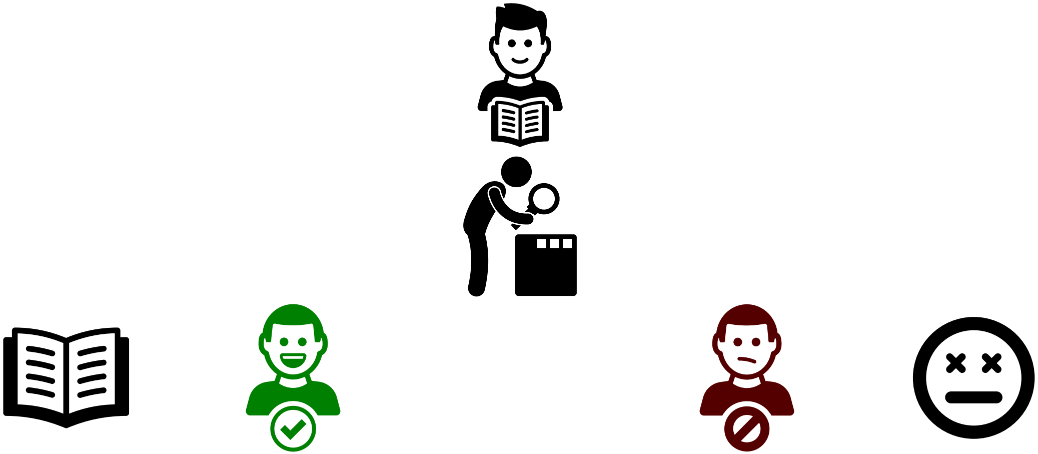
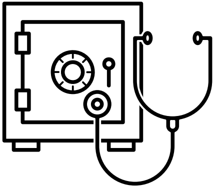


Side-channel Attacks

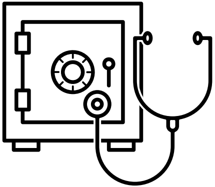
Side-channel Attacks

- Safe software infrastructure does not mean safe execution

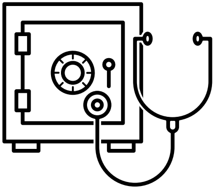


Side-channel Attacks

- Safe software infrastructure does not mean safe execution
- Information leaks because of the underlying hardware



Side-channel Attacks



- Safe software infrastructure does not mean safe execution
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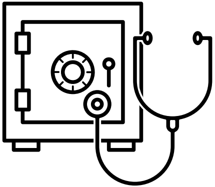
- Exploit unintentional information leakage by side-effects

Side-channel Attacks



- Safe software infrastructure does not mean safe execution
- Information leaks because of the underlying hardware
- Exploit unintentional information leakage by side-effects

Power consumption

Execution time

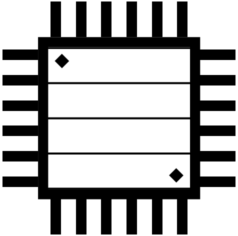
CPU caches

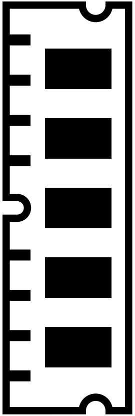
●●●

Caches and Cache Attacks

CPU Cache

```
printf("%d", i);
printf("%d", i);
```





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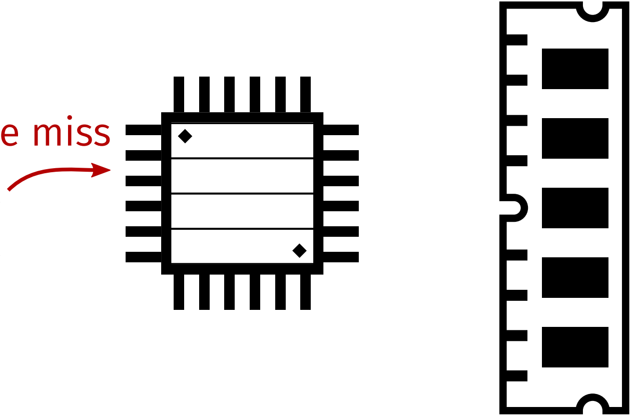

Cache miss

CPU Cache

```
printf("%d", i);
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```

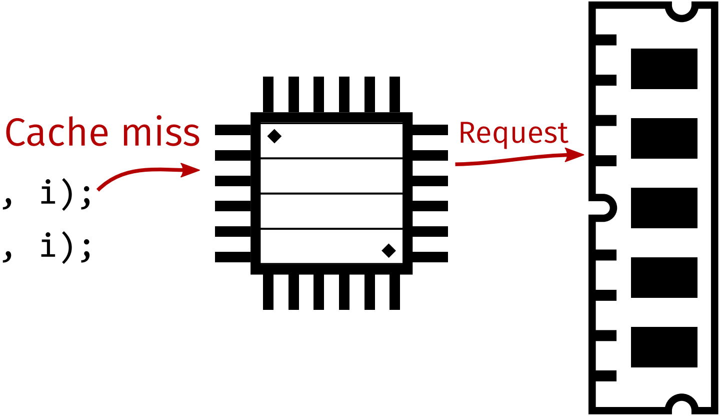

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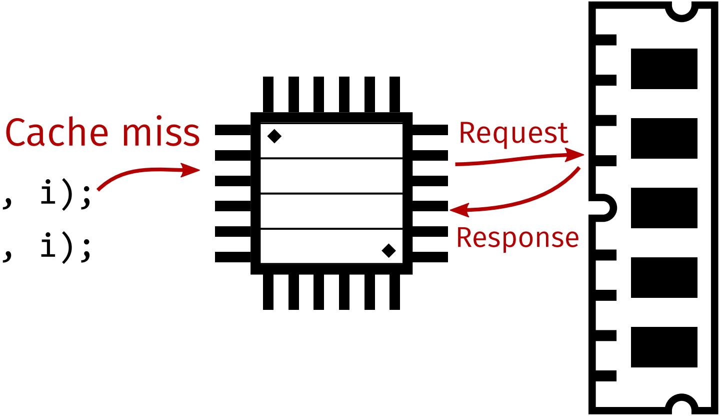

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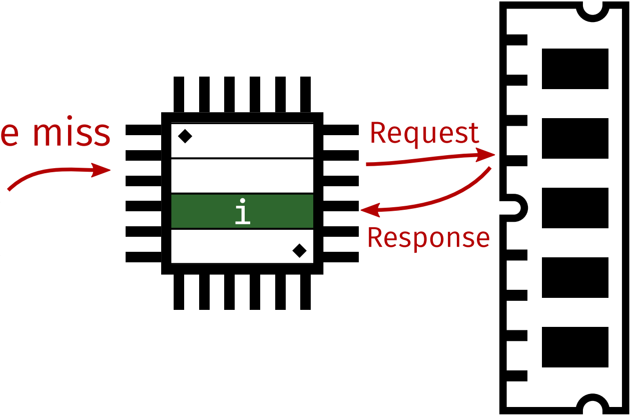


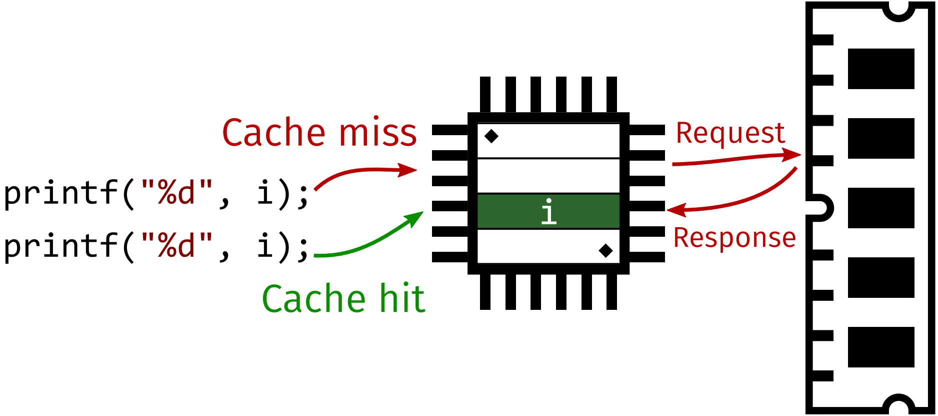
Cache miss

Request

Response

i

CPU Cache



```
printf("%d", i);
printf("%d", i);
```

Cache miss

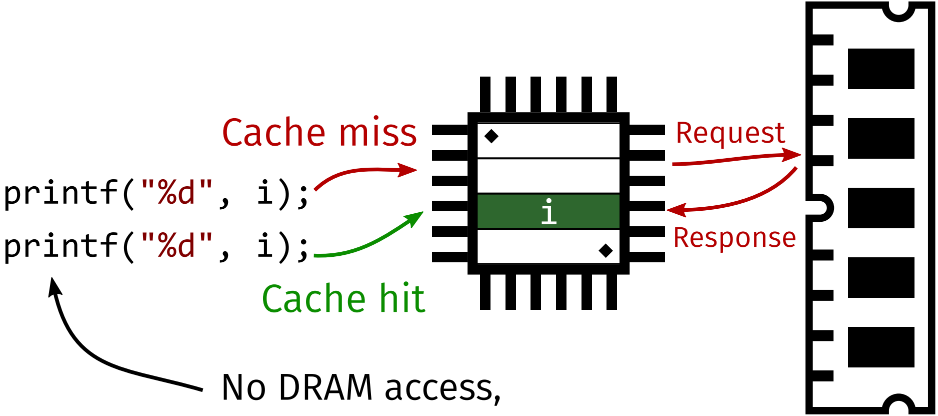
Cache hit

i

Request

Response

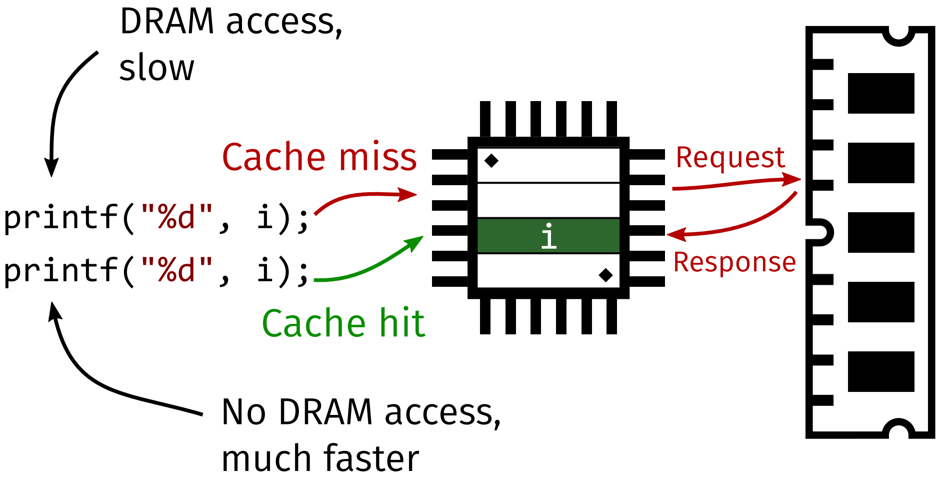
CPU Cache



```
printf("%d", i);
printf("%d", i);
```

No DRAM access,
much faster

CPU Cache



DRAM access, slow

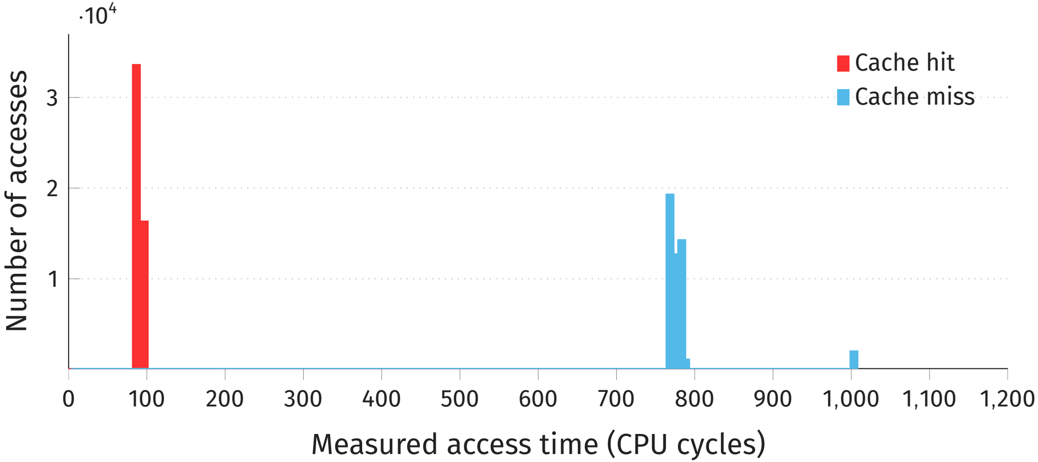
```
printf("%d", i);
printf("%d", i);
```

Cache miss

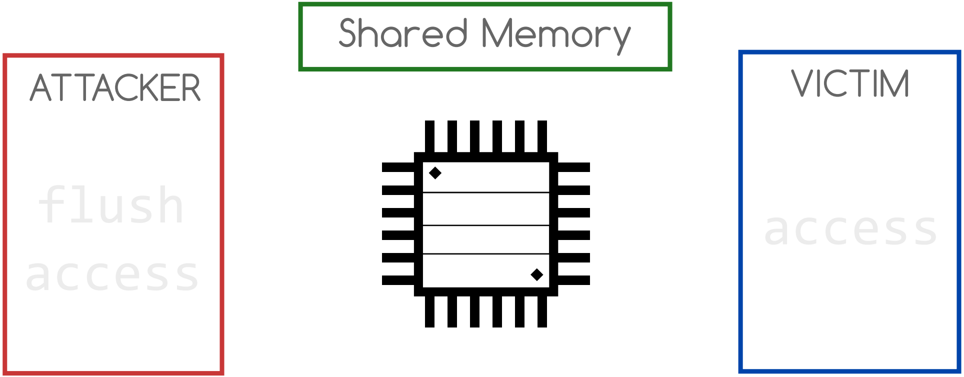
Cache hit

No DRAM access, much faster

Memory Access Latency



Flush+Reload



Shared Memory

ATTACKER

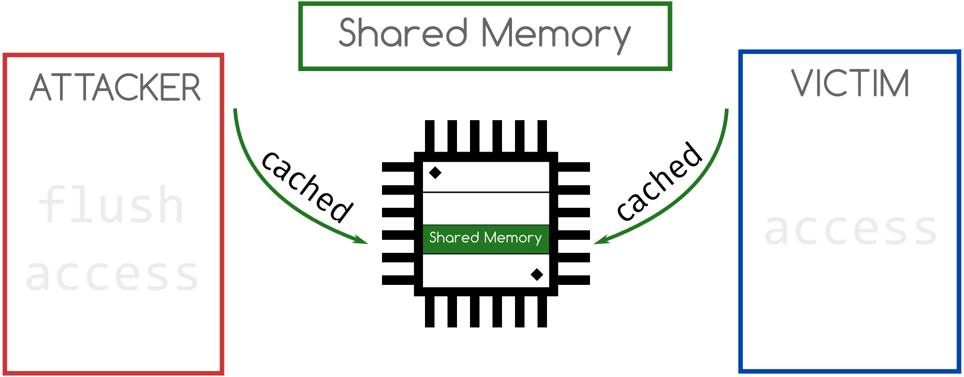
flush

access

VICTIM

access

Flush+Reload



Shared Memory

ATTACKER

flush

access

cached

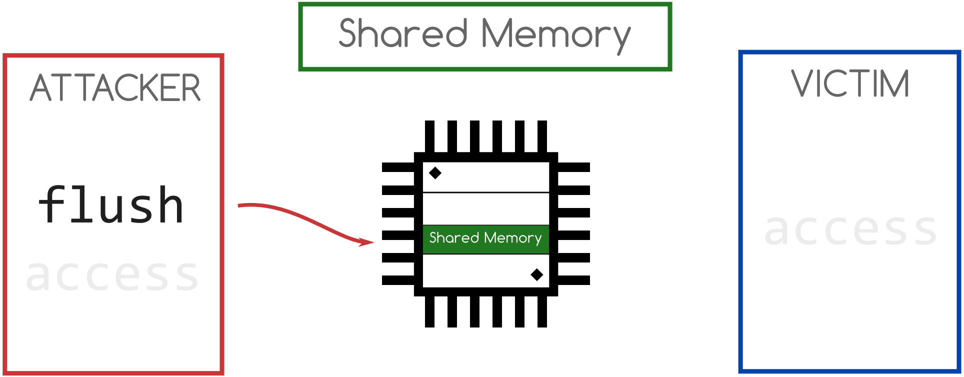
Shared Memory

cached

VICTIM

access

Flush+Reload



Shared Memory

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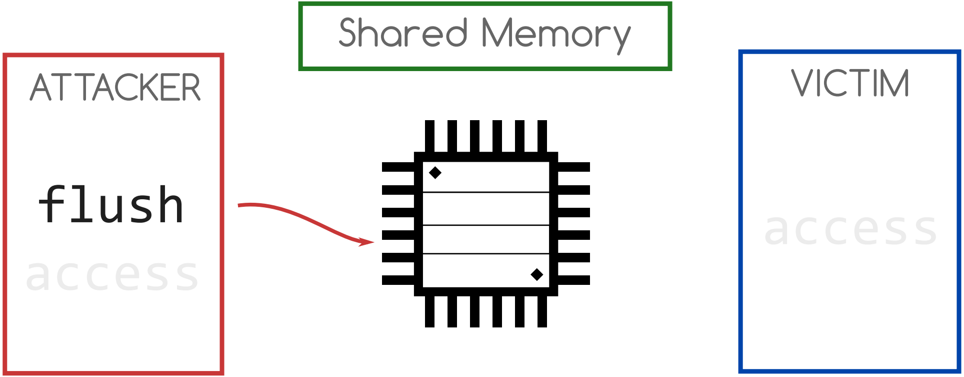
Flush+Reload



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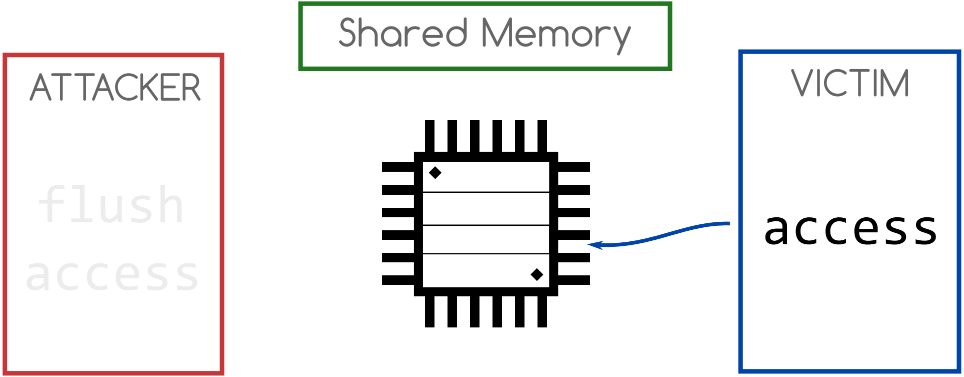

Shared Memory

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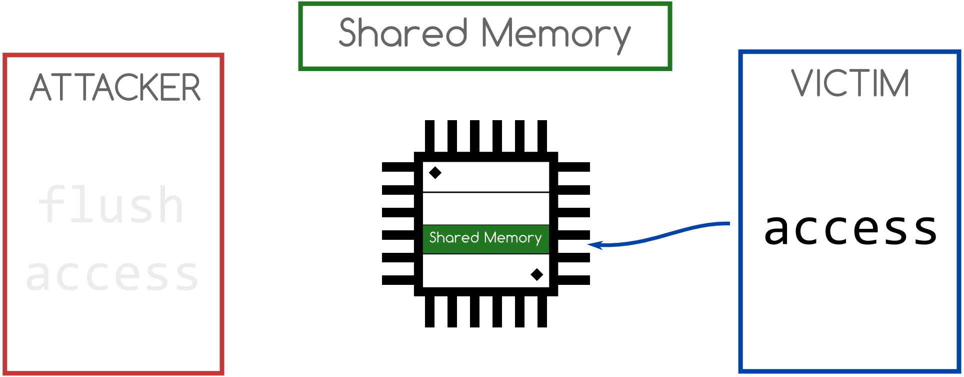


Shared Memory

ATTACKER

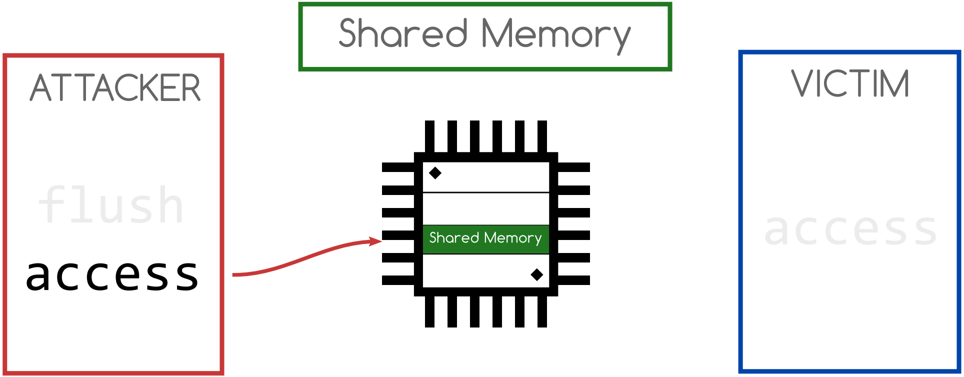
flush

access

VICTIM

access

Flush+Reload



Shared Memory

ATTACKER

flush

access

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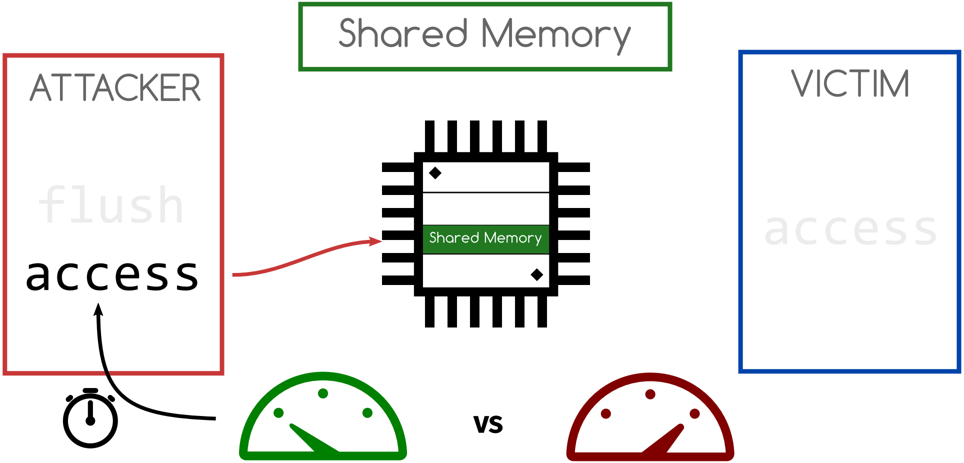
Flush+Reload



Shared Memory

ATTACKER

flush

access

Shared Memory

VICTIM

access

vs

Victim accessed (fast)

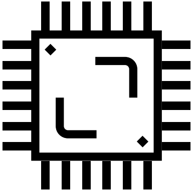
Victim did not access (slow)

Microarchitecture

Architecture and Microarchitecture

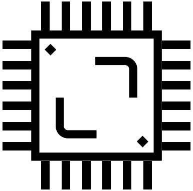
- Instruction Set Architecture (ISA) is an abstract model of a computer (x86, ARMv8, SPARC, ...)

Architecture and Microarchitecture



- Instruction Set Architecture (ISA) is an abstract model of a computer (x86, ARMv8, SPARC, ...)
- Serves as the interface between hardware and software

Architecture and Microarchitecture



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Architecture and Microarchitecture

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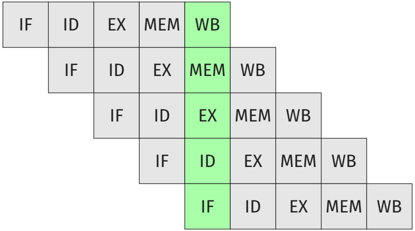
●●●

In-Order Execution



IF	ID	EX	MEM	WB				
	IF	ID	EX	MEM	WB			
		IF	ID	EX	MEM	WB		
			IF	ID	EX	MEM	WB	
				IF	ID	EX	MEM	WB

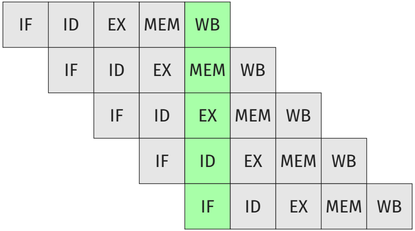
- Instructions are...
  - fetched (IF) from the L1 Instruction Cache

In-Order Execution

IF	ID	EX	MEM	WB				
	IF	ID	EX	MEM	WB			
		IF	ID	EX	MEM	WB		
			IF	ID	EX	MEM	WB	
				IF	ID	EX	MEM	WB

- Instructions are...
  - fetched (`IF`) from the L1 Instruction Cache
  - decoded (`ID`)

In-Order Execution



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- Instructions are...
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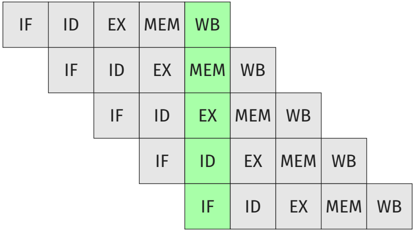
  - decoded (ID)
  - executed (EX) by execution units

In-Order Execution



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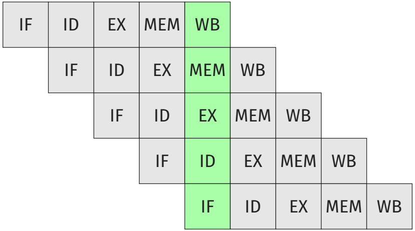
In-Order Execution



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- Instructions are...
  - fetched (`IF`) from the L1 Instruction Cache
  - decoded (`ID`)
  - executed (`EX`) by execution units
- Memory access is performed (`MEM`)
- Architectural register file is updated (`WB`)

In-Order Execution

- Instructions are executed in-order

In-Order Execution

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- Pipeline stalls when stages are not ready

In-Order Execution

- Instructions are executed in-order
- Pipeline stalls when stages are not ready
- If data is not cached, we need to wait

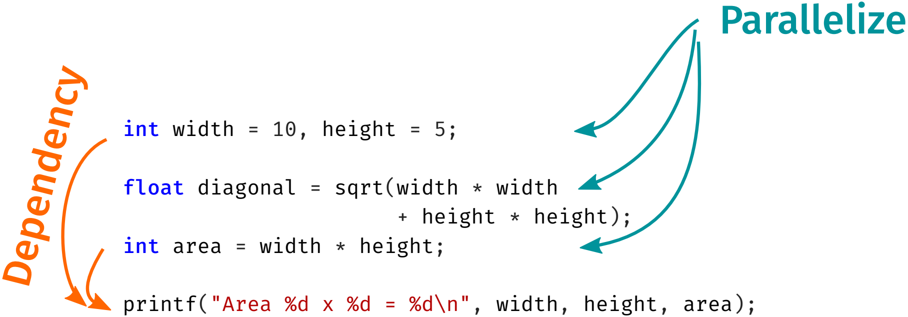
Out-of-order Execution

```c
int width = 10, height = 5;

float diagonal = sqrt(width * width
                      + height * height);
int area = width * height;

printf("Area %d x %d = %d\n", width, height, area);
```

Out-of-order Execution



Parallelize

Dependency

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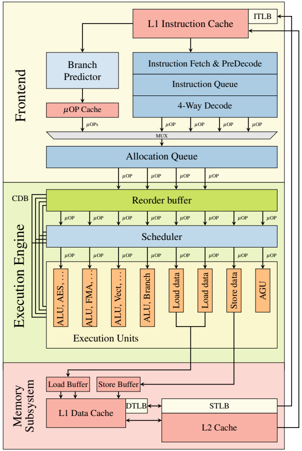

Instructions are

- fetched and decoded in the front-end

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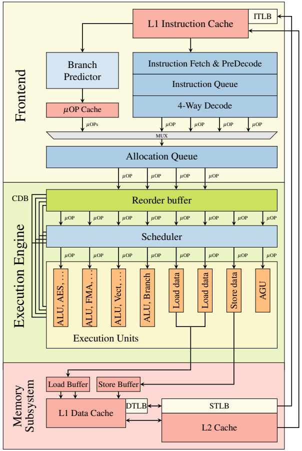

Instructions are

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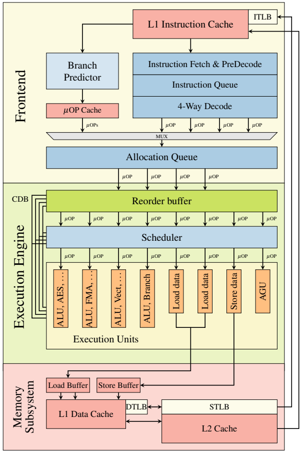
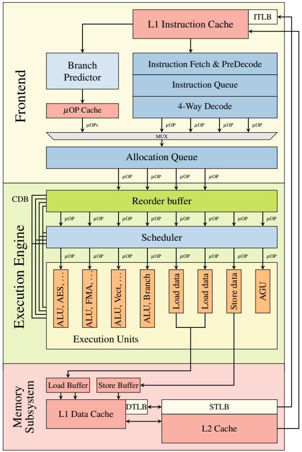
Out-of-Order Execution



Instructions are

- fetched and decoded in the front-end
- dispatched to the backend
- processed by individual execution units

Out-of-Order Execution



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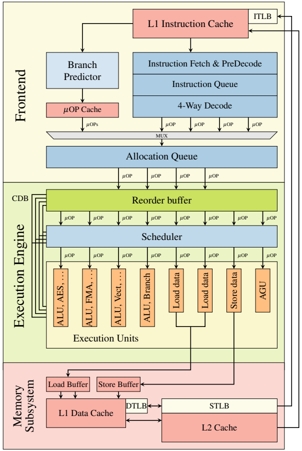

Instructions

- are executed out-of-order
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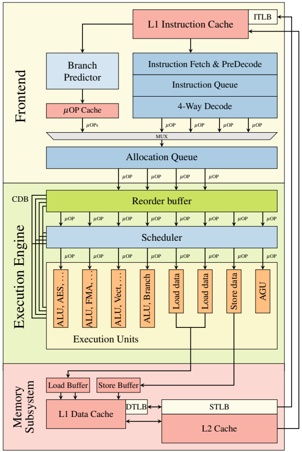
Out-of-Order Execution



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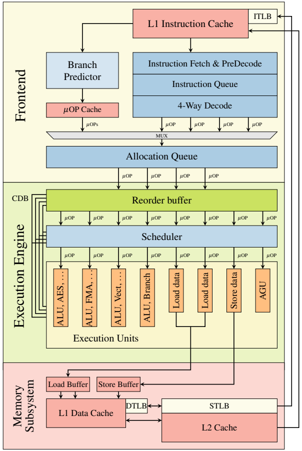

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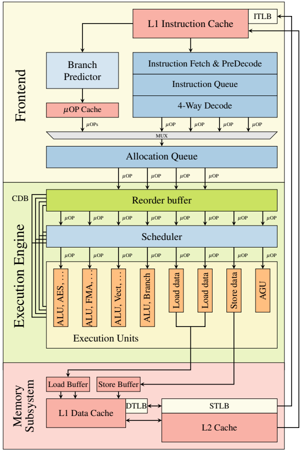

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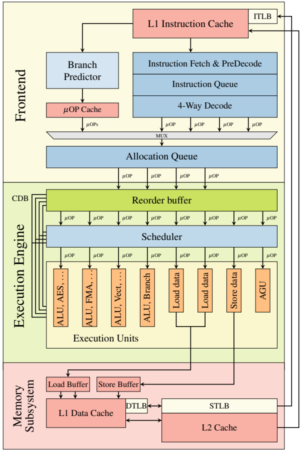

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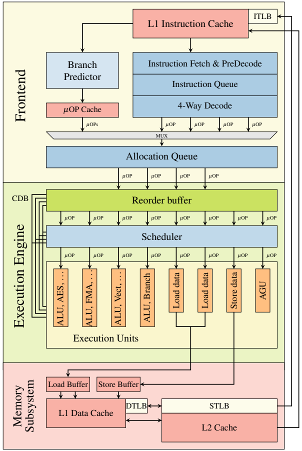

Instructions

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- Exceptions are checked during retirement
  - Flush pipeline and recover state

The state does not become architecturally visible but ...

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Building the Code

- New code

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*(volatile char*) 0;
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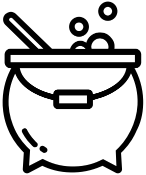
Building the Code



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```
warning: statement with no effect [-Wunused-value]
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```
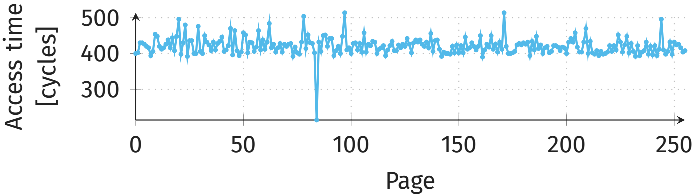

- Static code analyzer is still not happy

```
warning: Dereference of null pointer
        *(volatile char*)0;
```

- Flush+Reload over all pages of the array



Building the Code

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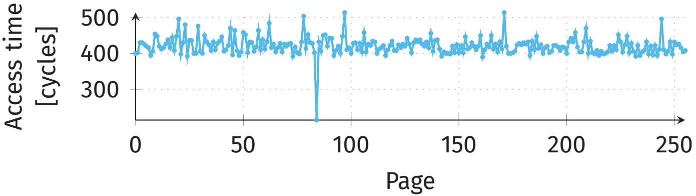

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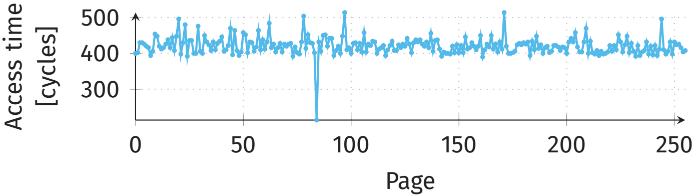

- “Unreachable” code line was actually executed
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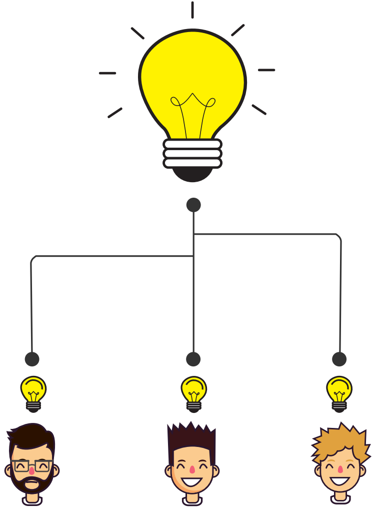
- Out-of-order instructions leave microarchitectural traces
  - We can see them for example in the cache
- Give such instructions a name: transient instructions
- We can indirectly observe the execution of transient instructions

Building the Code

December

3

Building the Code



Building the Code

- Add another layer of indirection to test

```
char data = *(char*) 0xffffffff81a000e0;
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Building the Code

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char data = *(char*) 0xffffffff81a000e0;
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```
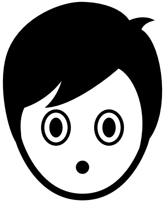

- Then check whether any part of `array` is cached

Building the Code



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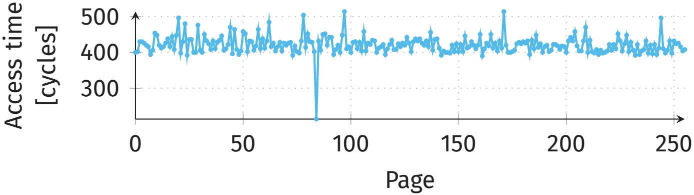

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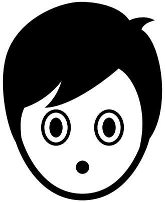
Building the Code



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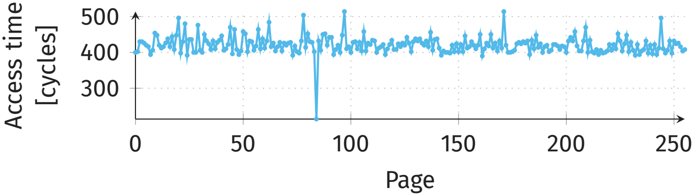

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MELTDOWN

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- Using out-of-order execution, we can read data at any address
- Index of cache hit reveals data
- Permission check is in some cases not fast enough
- Entire physical memory is typically accessible through kernel space

I SHIT YOU NOT
THERE WAS KERNEL MEMORY ALL OVER THE TERMINAL
STRONGBOW
memegenerator.net

Demo

Details: Exception Handling

- Basic Meltdown code leads to a crash (segfault)

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Fault Handling

Fault Suppression

Fault Prevention

Meltdown with Fault Suppression

- Intel TSX to suppress exceptions instead of signal handler

```c
if(xbegin() == XBEGIN_STARTED) {
  char secret = *(char*) 0xffffffff81a000e0;
  array[secret * 4096] = 0;
  xend();
}

for (size_t i = 0; i < 256; i++) {
  if (flush_and_reload(array + i * 4096) == CACHE_HIT) {
    printf("%c\n", i);
  }
}
```

Meltdown with Fault Prevention

- Speculative execution to prevent exceptions

```
int speculate = rand() % 2;
size_t address = (0xffffffff81a000e0 * speculate) +
                 ((size_t)&zero * (1 - speculate));
if(!speculate) {
  char secret = *(char*) address;
  array[secret * 4096] = 0;
}

for (size_t i = 0; i < 256; i++) {
  if (flush_and_reload(array + i * 4096) == CACHE_HIT) {
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  }
}
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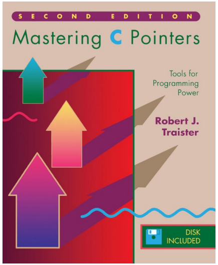
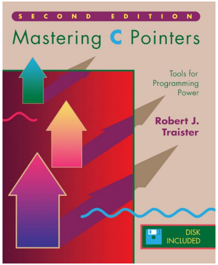
Make it faster



- Improve the performance with a NULL pointer dereference

Make it faster



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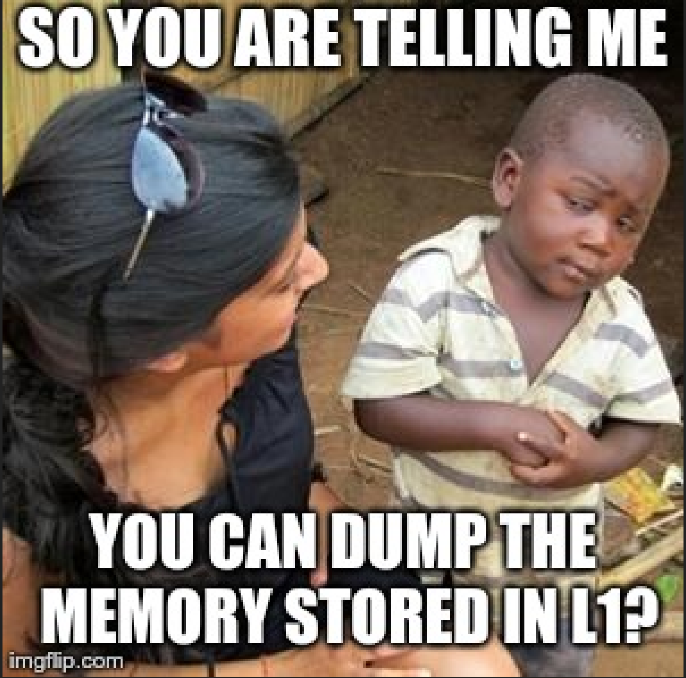
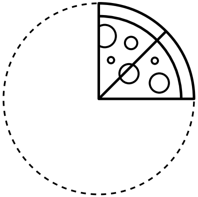

SO YOU ARE TELLING ME
YOU CAN DUMP THE MEMORY STORED IN L1?
imgflip.com

WHAT IF I TOLD YOU
YOU CAN LEAK THE ENTIRE MEMORY
imgflip.com

Uncached memory



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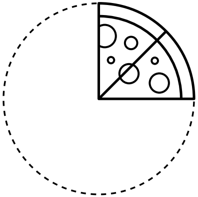

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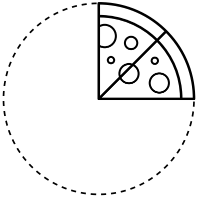

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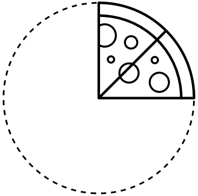

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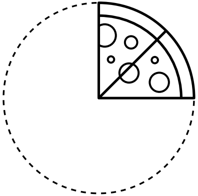

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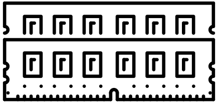
- Meltdown might implicitly cache the data

Uncachable memory

- Mark pages in page tables as UC (uncachable)

Uncachable memory



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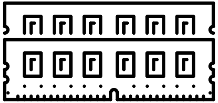

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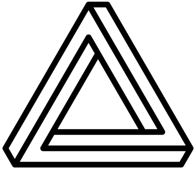
  - as they are shared between threads running on the same core

So you can dump the entire memory.

So you can dump the entire memory. But it takes ages?

Practical attacks



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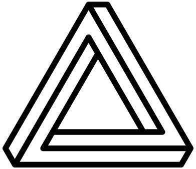
Practical attacks



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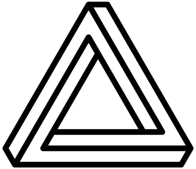

- Dumping the entire physical memory takes some time
  - Not very practical in most scenarios
- Can we mount more targeted attacks?

VeraCrypt

- Open-source utility for disk encryption

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VeraCrypt

- Open-source utility for disk encryption
- Fork of TrueCrypt
- Cryptographic keys are stored in RAM
  - With Meltdown, we can extract the keys from DRAM

Demo

Breaking KASLR

- De-randomize KASLR to access internal kernel structures

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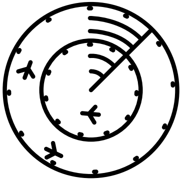
- Difference between the found address and the non-randomized base address is the randomization offset

Locating the victim process



- Linux manages all processes in a linked list

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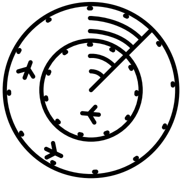

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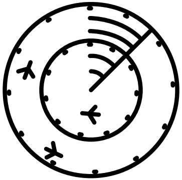

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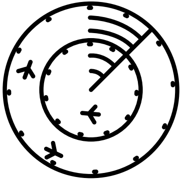
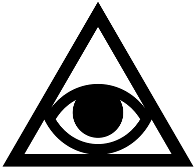


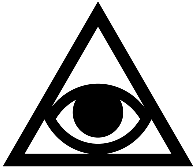
- Linux manages all processes in a linked list
- Head of the list is stored at `init_task` structure
    - At a fixed offset that varies only among kernel builds
- Each task list structure contains a pointer to the next task and
    - PID of the task
    - name of the task
    - Root of the multi-level page table

Dumping memory content



- Resolve physical address using paging structures

Dumping memory content



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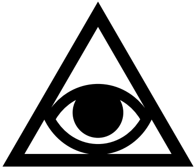

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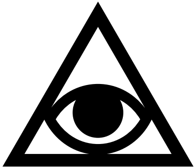

- Resolve physical address using paging structures
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- Enumerate all mapped pages and dump entire process memory
- Location of the key known, we can just dump the key directly

Final steps

- `aeskeyfind` to extract AES keys from the memory dump

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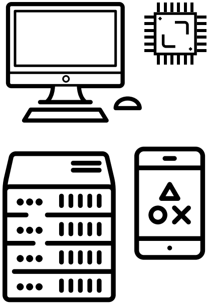
- Affects every application that stores its secret in DRAM

Who is affected?

Affected by Meltdown



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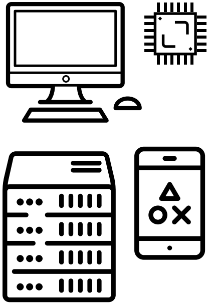

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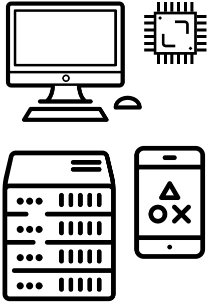

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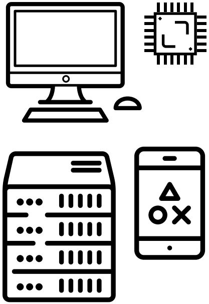

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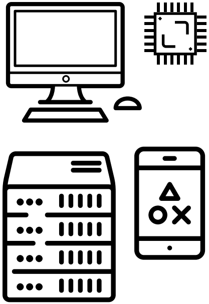

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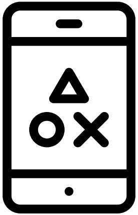

- But there are other CPU manufacturers as well ...

Samsung Galaxy S7

Samsung Galaxy S7

- Exynos Mongoose M1 CPU Architecture

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SAMSUNG GALAXY S7

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Demo

Samsung Galaxy S7

SAMSUNG GALAXY S7

- Luckily they already fixed it

Samsung Galaxy S7

Samsung Galaxy S7

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Samsung Galaxy S7

Samsung Galaxy S7

- Luckily they already fixed it
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Affected by Meltdown

- But there are other CPU manufacturers as well ...
- ...which are affected
- Need to evaluate the attack on other CPUs as well
- Notify the users ...
- ...and custom ROM developers, e.g., LineageOS

But wait, what about privileged registers?

Variant 3a

- ARM found a closely related Meltdown variant

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- ARM Cortex-A15, Cortex-A57 and Cortex-A72 are vulnerable
- Impact: breaking KASLR and pointer authentication

Demo

Variant 3a

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- Rogue System Register Read (RSRE) (CVE-2018-3640)

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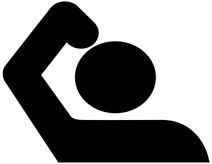

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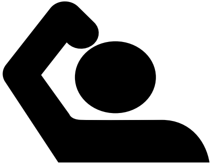

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→ does not make the entire thing a side-channel attack

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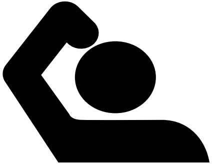

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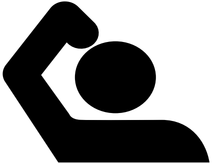

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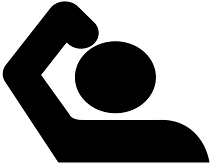

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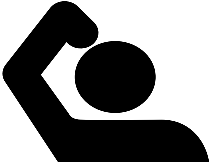

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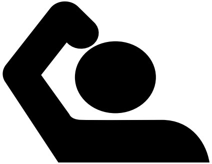

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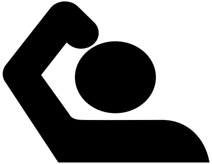

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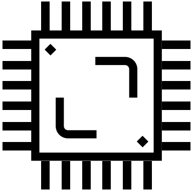
→ Actual problem: fetching & using real values for instructions after faulting ones

How can this all be fixed?

Meltdown Mitigation



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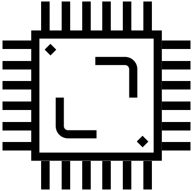
Meltdown Mitigation



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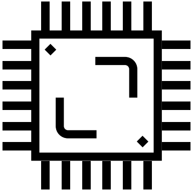

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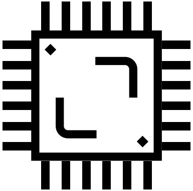

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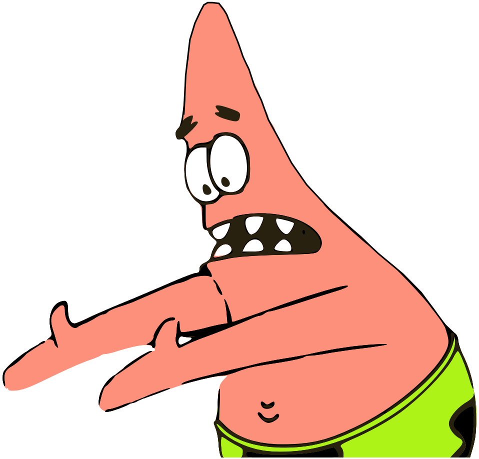
- Fix the hardware → long-term solution
- Can we fix it in software?

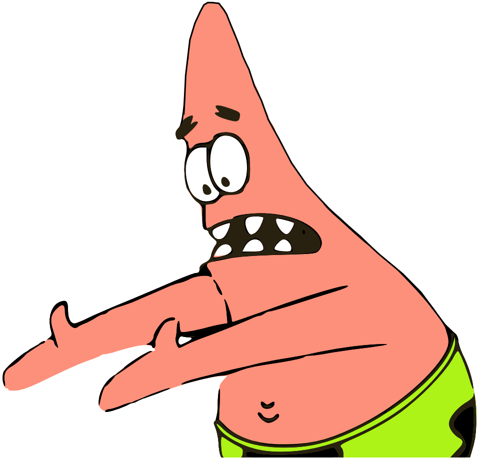
Meltdown Mitigation

- Kernel addresses in user space are a problem



Meltdown Mitigation

- Kernel addresses in user space are a problem
- Why don't we take the kernel addresses...



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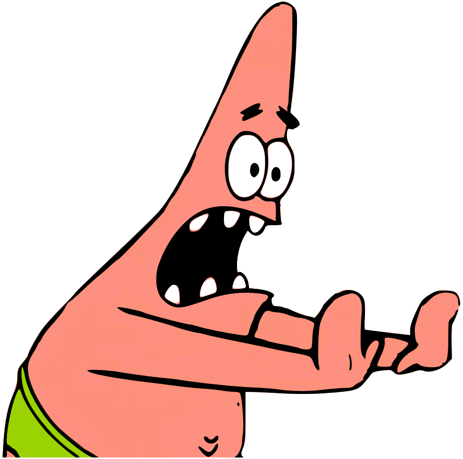
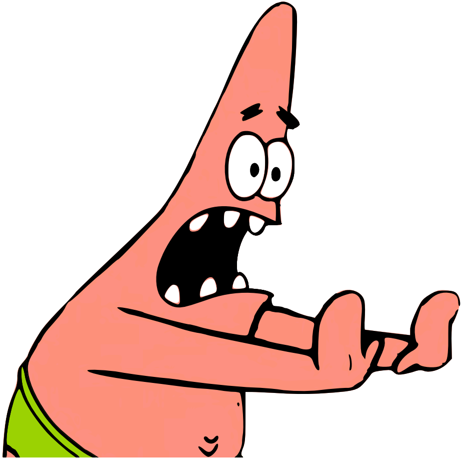


- …and remove them if not needed?

Meltdown Mitigation



- ...and remove them if not needed?
- User accessible check in hardware is not reliable

Meltdown Mitigation

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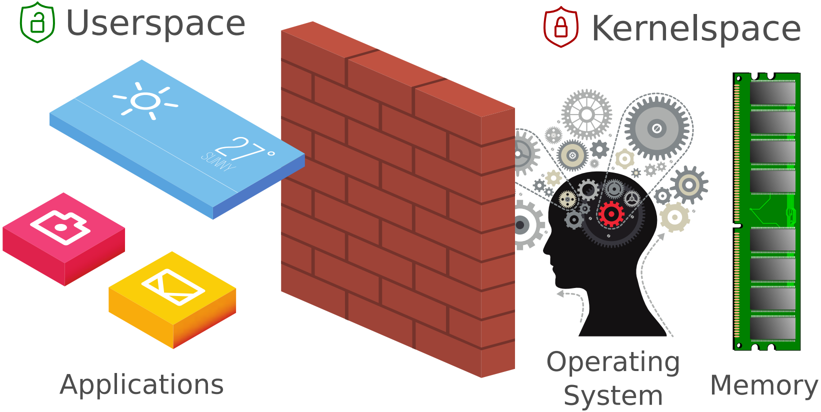
- Memory which is not mapped cannot be accessed at all

KAISER



Userspace

Kernelspace

Applications

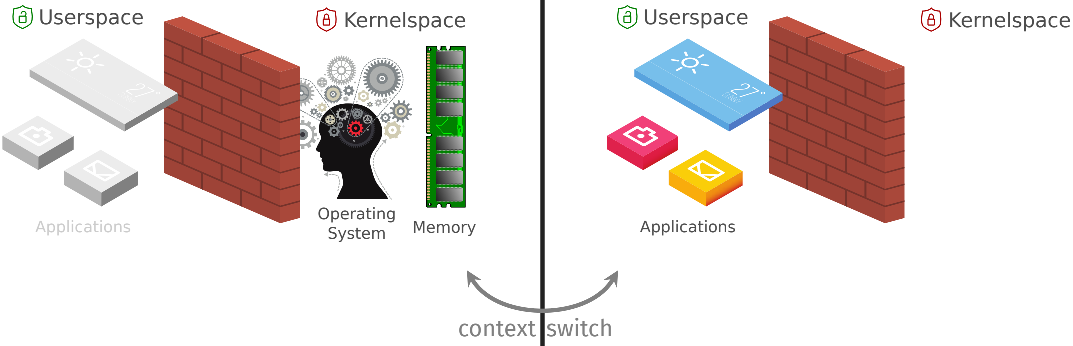
Operating System

Memory

KAISER

Kernel View

User View



Userspace

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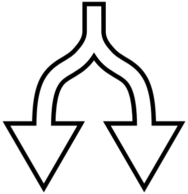
context switch

KAISER



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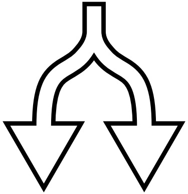

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- Inadvertently defeats Meltdown as well
- PoC implementation for the Linux kernel

KAISER

- Hardware interrupt while running in user mode
  - Kernel needs to deal with interrupt but does not exist anymore in address space
  - Traps, NMI, system calls, ...
- Must map some kernel code in user space

KAISER

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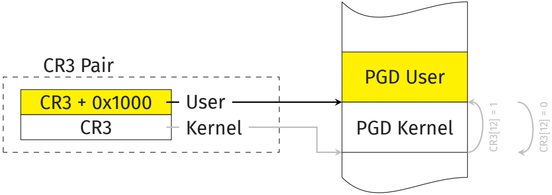

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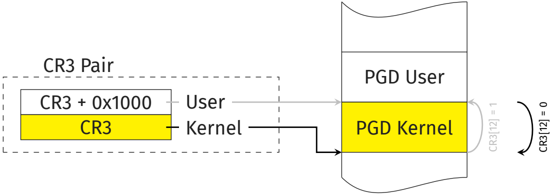

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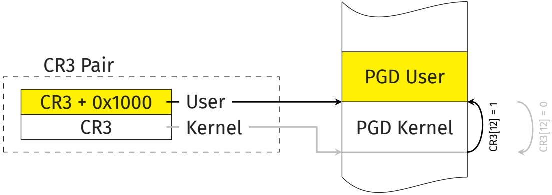
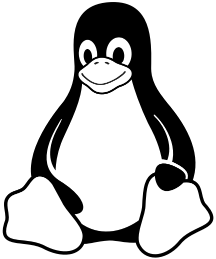


Kernel Page-table Isolation



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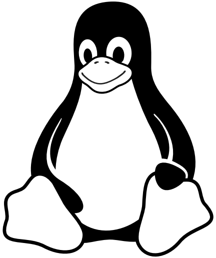

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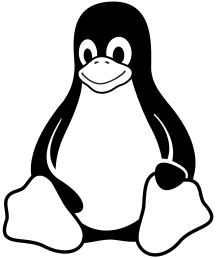


- Intel and others improved KAISER
- Merged it into upstream as KPTI (Kernel Page-table Isolation)
- Kernel patches are available for arm64 as well

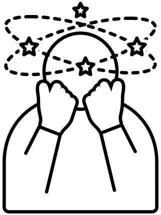
Apple

- Apple released updates in iOS 11.2, macOS 10.13.2 and tvOS 11.2 to mitigate Meltdown
- Boot option: `-no-shared-cr3`
  - Unmaps the user space while running in kernel mode
  - But not vice versa

KVA Shadow

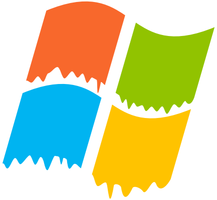
- Kernel Virtual Address (KVA) Shadow
- Meltdown Mitigation for Microsoft Windows

Implementing



- Introducing such a fundamental change to the operating system is extremely challenging
- Our PoC implementation contained many bugs as well

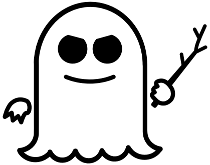
Total Meltdown



- Discovered by Ulf Frisk (@ulffrisk) in the 2018-02 security update
  - CVE-2018-1038
- Modified the PML4 entry of `0x1ed` to allow to access page from user-mode
- On Windows 7 and Server 2018 R2: Self-Referencing Entry
- Allows to read and modify entire physical memory

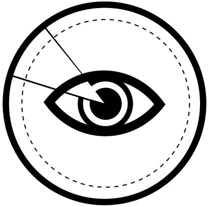
What now?

Future



- More attacks exploiting performance optimizations in hardware
  - New variants are disclosed frequently

A unique chance



A unique chance to

- rethink processor design
- grow up, like other fields (car industry, construction industry)

Proof-of-Concept

You can find our proof-of-concept implementation on:

- `https://github.com/IAIK/meltdown`

Conclusion

- Underestimated microarchitectural attacks for a long time
- Meltdown exploit performance optimizations
  - Allow to leak arbitrary memory
- Countermeasures come with a performance impact
- Find trade-offs between security and performance

Moritz Lipp (@mlqxyz)

Michael Schwarz (@misc0110)

Daniel Gruss (@lavados)

Meltdown

Basics, Details, Consequences

Black Hat USA 2018
9 August, 2018 - Las Vegas, NV, USA

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